APPLICATION		REVISIONS			
NEXT ASSY	FINAL ASSY	LTR	DESCRIPTION	DATE	APPROVED
		–	PRODUCTION RELEASE/E.O. 29226	3/19/93	D. Goodale
		A	E.O. 29434	6/3/93	D. Goodale
		B	E.O. 29653	11/30/93	D. Goodale
		C	E.O. 36743, Revised and Redrawn	2/12/02	D. Goodale

Specification

4 x 20 Daystar Nova LCD Module

With

Parallel Data Input Option

Model 03805–06–0100

REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C				
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

REVISION STATUS

PROJ. NO. 411	**CONTRACT**		**INDUSTRIAL ELECTRONIC ENGINEERS, INC.** **VAN NUYS, CALIFORNIA**
	DRAWN R. January 3–19–93		PARALLEL DATA INPUT 4 X 20 LCD MODULE
	CHECK		
	APPROVED D. Goodale 3-19-93	**SIZE** A	**CODE IDENT NO.** 05464 / **S03805–06–0100**
	APPROVED	SCALE	SHEET 1 OF 20

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1.0 GENERAL INFORMATION

1.1 Introduction

This specification describes the parallel interface Daystar Nova model 03805–06–0100, a 4–line supertwist liquid crystal display (LCD) with 20 characters per line.

Model Number Designation System

03805	–	06	–	0	1	0	0
Reflective STN LCD		4x20 Format		Reserved	1 = Parallel Data Input * 2 = Serial Data Input	0 = No Backlight	0 = Color N/A

* Parallel standard, Serial optional

1.2 Application

Daystar Nova modules provide alphanumeric information which is easily readable in high ambient light or in darkness with optional backlight. The low power requirements of the modules make them suitable for portable battery operated equipment. The wide operating temperature range (–30° to +80°C) is ideal for most outdoor applications. The choice of a preferential viewing hemisphere is not necessary because of the excellent wide angle viewing characteristics of the new Super Bi–refringent Effect (SBE) liquid crystal cell used in this display.

For applications where the display is remotely located up to 50 feet from the host processor, the serial data input option should be used. The serial option model is described in IEE specification S03805–06–0200.

1.3 Description

The Daystar Nova module is a self–contained 1/16 multiplexed unit. A simple parallel interface is provided and can be configured as either 4 or 8 bits. The on–board microprocessor controls the display, multiplexing and character decoding. The temperature compensation circuitry guarantees that the viewing characteristics are optimized for all temperatures.

The SBE liquid crystal cell used in this display has a golden–green background with dark blue–black characters.

The on–board character generator ROM generates 192 types of alphanumeric, numeric, katakana characters and symbols. In addition, a character generator RAM allows the user to define eight additional characters.

A variety of high level functions allow the programmer to operate the display with simple and straightforward software routines. One such feature automatically increments the character display position after each character is written.

A single +5 Volt nominal power supply is required for operation of the LCD module. The unit operates from 4.50 Volts to 5.50 Volts. The typical power requirement for the module is 40mW.

The module weighs 6.3 oz. (179 grams).

2.0 LOGICAL STRUCTURE AND FUNCTION

2.1 Module Block Diagram

Figure 1 illustrates the major components of the Daystar Nova module. The microprocessor controls all multiplexing and character decoding. The temperature compensation network optimizes both viewing and contrast ratio for the display over all operating temperatures.

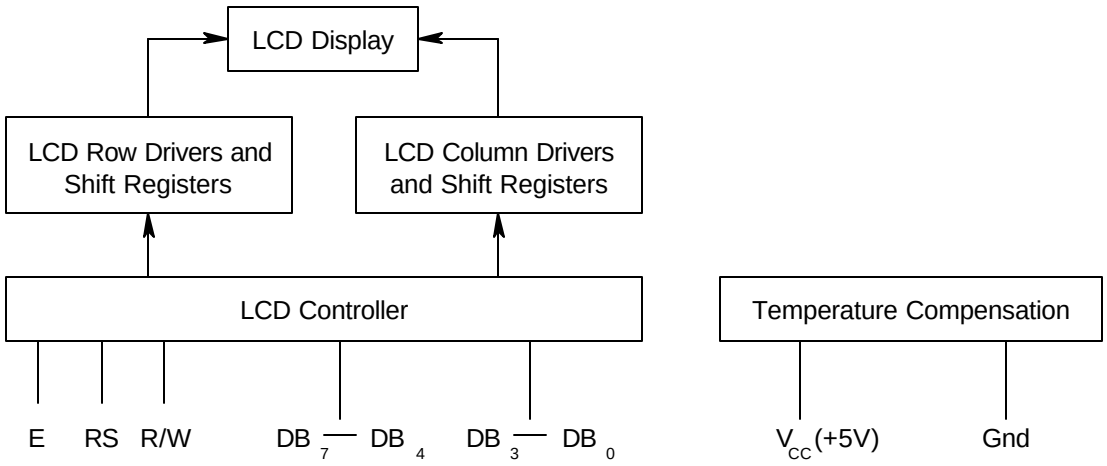

Figure 1 Module Block Diagram

2.1.1 Signal Description

Signal Name	Number Of Lines	Input/Output	Connected
RS	1	I	MPU
R/W	1	I	MPU
E	1	I	MPU
DB_4–DB_7	4	I/O	MPU
DB_0–DB_3	4	I/O	MPU
V_{CC}	2	–	Power
GND	7	–	–

2.2 LCD Controller

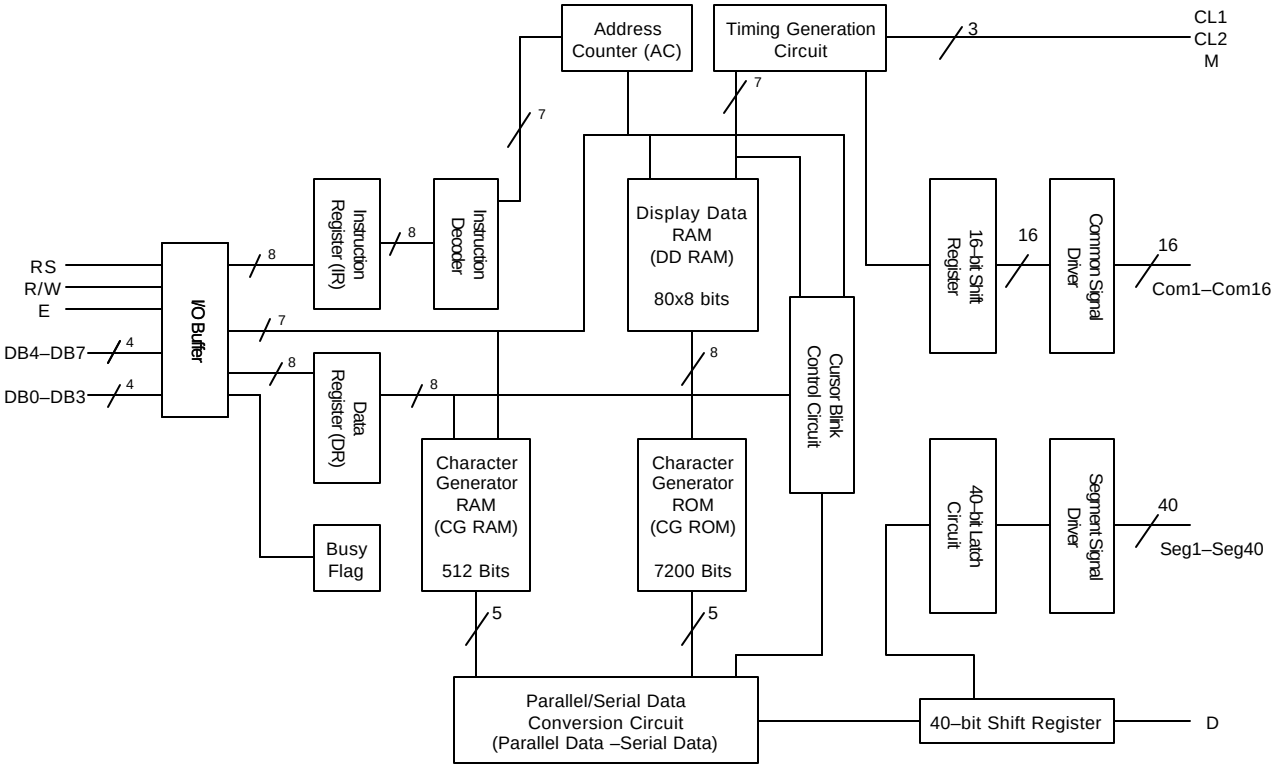

Figure 2 LCD Controller Block Diagram

2.2.1 Instruction Register (IR)

The IR stores instruction codes such as display clear and cursor shift, and address information of the display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU, but not read.

2.2.2 Data Register (DR)

The DR temporarily stores data to be written into or read from the DD RAM or the CG RAM.

2.2.3 Busy Flag

When the Busy Flag is a "1", the module is in an internal operating mode and ignores any additional instructions (Refer to Read Busy Flag and Address instruction).

2.2.4 Address Counter (AC)

The AC determines the address of the DD RAM or CG RAM in which new data is stored. After writing into (or reading from) the DD RAM or CG RAM, the AC is incremented or decremented as defined by the Increment/Decrement bit (Refer to Entry Mode Set instruction).

2.2.5 Display Data RAM (DD RAM)

The DD RAM contains 80 X 8 bits and represents 80 characters. The relationship between the DD RAM

address and position of the characters in the display can be controlled by the user (Refer to Entry Mode Set and Cursor or Display Shift instructions).

2.2.6 Character Generator ROM (CG ROM)

The CG ROM generates character patterns of 5 X 7 dots from 8 bit character codes. The 192 5 X 7 dot matrix characters are illustrated in Figure 3.

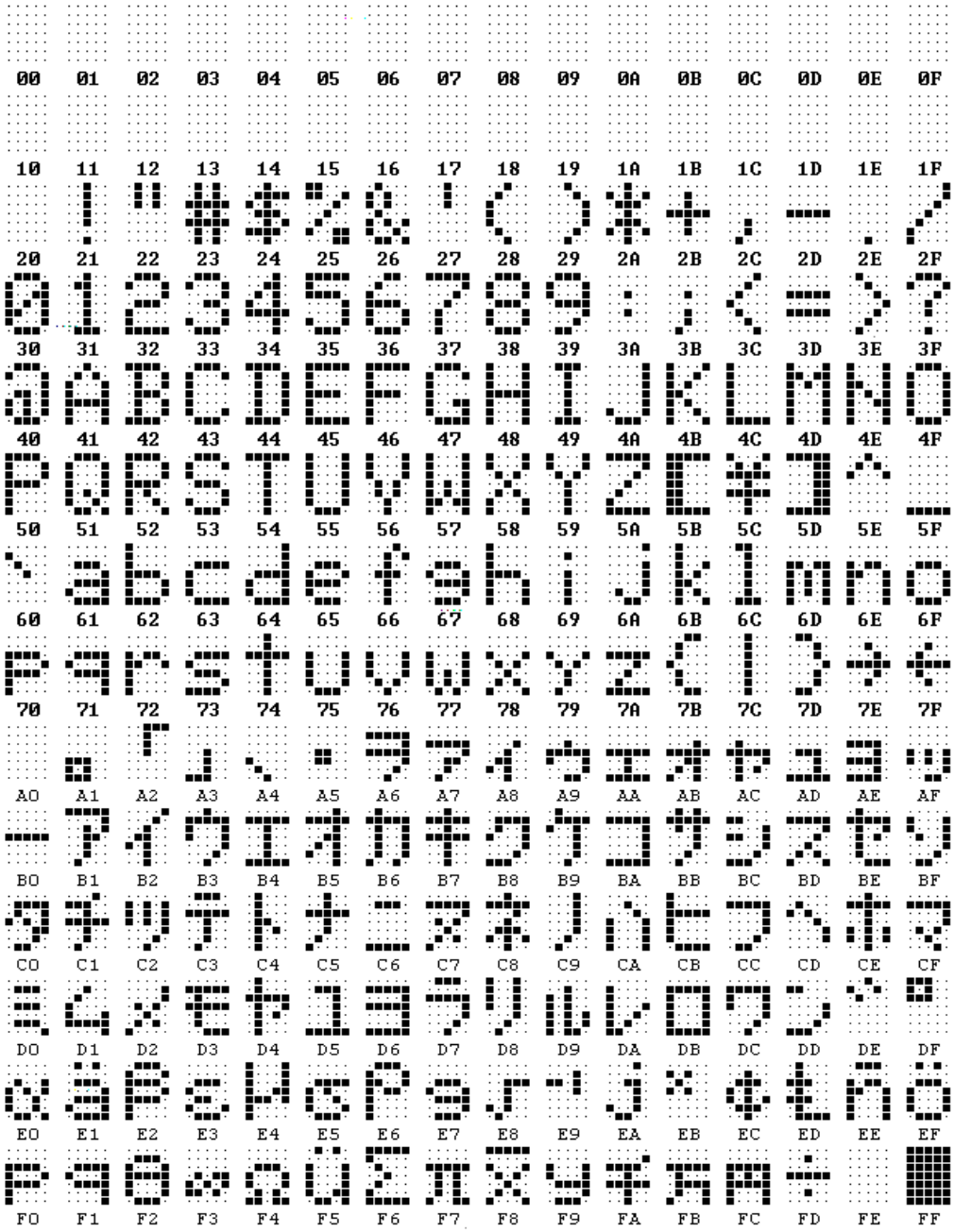

Figure 3 Correspondence Between Character Codes and Character Patterns

Note: Addresses 00h through 0Fh are reserved for CG RAM Addressing. Addresses 10h through 1Fh and 80h through 9Fh are not used.

2.2.7 Character Generator RAM (CG RAM)

The CG RAM allows the user to define 8 types of 5 X 7 character patterns. Figure 4 shows the relationship

between CG RAM addresses and data patterns (Refer to Set CG RAM Address and Write to CG or DD RAM instructions).

Character Codes (DD RAM Data)									CG RAM Address							Character Patterns (CG RAM Data)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0		7	6	5	4	3	2	1	0	
←Higher Order Bits Lower Order Bits→									←Higher Order Bits Lower Order Bits→							←Higher Order Bits Lower Order Bits→								
												0	0	0		*	*	*	1	1	1	1	0	
												0	0	1					1	0	0	0	1	
												0	1	0					1	0	0	0	1	Character
												0	1	1					1	1	1	1	0	Pattern
0	0	0	0	*	0	0	0		0	0	0	1	0	0					1	0	1	0	0	Example
												1	0	1					1	0	0	1	0	
												1	1	0					1	0	0	0	1	
												1	1	1		*	*	*	0	0	0	0	0	←Cursor

Figure 4 Relationship Between CG RAM Address, Character Codes (DD RAM) and Character Patterns (CG RAM Data)

NOTES:

1) The CG RAM consists of 64 bytes. Any bytes not used for character pattern information can be used for general purpose data RAM. The 5, 6 and 7 bits are never used for character pattern information and are always available for use.
2) The 0, 1 and 2 bits of character code correspond to the 3, 4 and 5 bits of the CG RAM address.
3) The 0, 1 and 2 bits of the CG RAM address specify the row of the character pattern.
4) The 8th row of the character pattern corresponds to the cursor character pattern. If any bit in the row is "1", then the corresponding cursor bit is a "1" regardless of cursor position. (For most applications, the data should be "0" in this row, which allows for normal cursor operation on the character.)
5) Since bit 3 is a "don't care", two character codes represent the same special character. For example, a character code of 07 (hexadecimal) selects the same character pattern as OF (hexadecimal).

2.2.8 Parallel/Serial Data Conversion Circuitry, Timing Generator Circuitry

These blocks control the interface to the LCD drivers.

3.0 OPERATION

3.1 Instruction Set

Instruction	Code										Description	Execution Time (Max)
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM to 0	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAN counter to 0. If the display has been shifted, characters are returned to their initial positions. DD RAM contents remain unchanged.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets shift register direction and cursor movement direction which occur during data read and write operations	40µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Turns ON/OFF the entire display (D), cursor) and cursor blink attribute (B).	40µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor or shifts entire display one position. DD RAM contents are unchanged.	40µs
Function Set	0	0	0	0	1	DL	1	0	*	*	Sets Interface Data Length.	40µs
Set CG RAM Address	0	0	0	1							Sets CG RAM address. CG RAM data is sent or received after this is set.	40µs
Set DD RAM Address	0	0	1								Sets DD RAM address. DD RAM data is sent or received after this is set.	40µs
Read Busy Flag and Address	0	1	BF								Reads Busy Flag (BF) and Address Counter	0µs
Write Data to CG or DD RAM	1	0									Writes data into CG RAM or DD RAM.	40µs
Read Data from CG or DD RAM	1	1									Reads data from CG RAM or DD RAM.	40µs

I/D=1:	Increment	DD RAM:	Display Data RAM
I/D=0:	Decrement	CG RAM:	Character Generator RAM
S=1:	Enable Shift Operation	A_{CG}	CG RAM Address
S/C=1:	Shift Display	A_{DD}	DD RAM Address
S/C=0:	Shift Cursor		(Corresponds to cursor address)
R/L=1:	Shift Right	AC	Address Counter
R/L=0:	Shift Left		(used for both CG and DD RAM)
DL=1:	8–bit operation	*	Don't Care
DL=0:	4–bit operation		
BF=1:	Operating internally		
BF=0:	Can accept instruction		

Figure 5 LCD Controller Instruction Set

3.2 Power Up Instructions Sequence

Upon power up, the Daystar Nova module is set to a default mode of operation. Under some power up circumstances, the default mode may be improperly set. Consequently, the following instructions should always be executed in the host systems initialization routine.

Step	Operation
1	Function Set for 8 bits
2	Repeat, Function Set for 8 bits
3	Function Set
4	Clear Display
5	Entry Mode Set
6	Display On/Off Control

STEP	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	0	0	0	0	1	1	*	*	*	*
2	0	0	0	0	1	1	*	*	*	*
3	0	0	0	0	1	DL	1	0	*	*
4	0	0	0	0	0	0	0	0	0	1
5	0	0	0	0	0	0	0	1	I/D	S
6	0	0	0	0	0	0	1	D	C	B

Refer to instruction set for values of DL, I/D, S, D, C and B. (* Don't care)

3.3 Instructions Affecting the Relationship of Display Position, Cursor, and DD RAM Address

The DD RAM contains the 8 bit character codes of the 40 characters displayed on the Daystar Nova LCD. The Cursor or Display Shift instruction and the Write to DD RAM and Entry Mode instructions affect the relationship between DD RAM address and display position. Figures 6 to 10 illustrate the effects of these instructions.

00*	01	02	03	04	05	06	07	08	09	0A		0E	0F	10	11	12	13	
40	41	42	43	44	45	46	47	48	49	4A		4E	4F	50	51	52	53	
14	15	16	17	18	19	1A	1B	1C	1D	1E		22	23	24	25	26	27	
54	55	56	57	58	59	5A	5B	5C	5D	5E		62	63	64	65	66	67	

* = Cursor

Figure 6 Initial Conditions on Power Up

01	02	03	04	05	06	07	08	09	0A	0B		0F	10	11	12	13	14
41	42	43	44	45	46	47	48	49	4A	4B		4F	50	51	52	53	54
15	16	17	18	19	1A	1B	1C	1D	1E	1F		23	24	25	26	27	00*
55	56	57	58	59	5A	5B	5C	5D	5E	5F		63	64	65	66	67	40

* = Cursor

Figure 7 Display Shift Left from Initial Conditions

27	00*	01	02	03	04	05	06	07	08	09		0D	0E	0F	10	11	12
67	40	41	42	43	44	45	46	47	48	49		4D	4E	4F	50	51	52
13	14	15	16	17	18	19	1A	1B	1C	1D		21	22	23	24	25	26
53	54	55	56	57	58	59	5A	5B	5C	5D		61	62	63	64	65	66

* = Cursor

Figure 8 Display Shift Right from Initial Conditions

01*	02	03	04	05	06	07	08	09	0A	0B		0F	10	11	12	13	14
41	42	43	44	45	46	47	48	49	4A	4B		4F	50	51	52	53	54
15	16	17	18	19	1A	1B	1C	1D	1E	1F		23	24	25	26	27	00#
55	56	57	58	59	5A	5B	5C	5D	5E	5F		63	64	65	66	67	40

* = Cursor
# = Last Character Entered

Figure 9 Load Character with S=1, I/D=0 from Initial Conditions

27*	00#	01	02	03	04	05	06	07	08	09		0D	0E	0F	10	11	12
67	40	41	42	43	44	45	46	47	48	49		4D	4E	4F	50	51	52
13	14	15	16	17	18	19	1A	1B	1C	1D		21	22	23	24	25	26
53	54	55	56	57	58	59	5A	5B	5C	5D		61	62	63	64	65	66

* = Cursor
# = Last Character Entered

Figure 10 Load Character with S=1, I/D=1 from Initial Conditions

3.4 Instructions Affecting Custom Characters

The module allows the user to define 8 unique special characters. The pattern of the characters is stored in the CG RAM. The relationship between the CG RAM address and the character pattern is illustrated in Figure 4. The Read Data from CG RAM, Write Data to CG RAM, and Set DD RAM instructions provide for easy programmability.

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Rating

Power Supply Voltage (V_{CC})	–0.3 to +6.5 V_{DC}
Input Voltage	–0.3 to +V_{CC} +0.3 V_{DC}

4.2 Normal Operating Rating

Power Supply Voltage (V_{CC})	+5.0 Volts ±10%
Power Supply Current	9 mA $\pm$ 3 mA

4.3 Electrical Characteristics (V_{CC} = 5V ±10%)

Item	Symbol	Condition	Min	Max	Unit
Input "High" Voltage	V_{IH}	2.2	V_{CC}	V	
Input "Low" Voltage	V_{IL}	–0.3	0.6	V	
Output "High" Voltage (TTL)	V_{OH1}	I_{OH} = 0.205 mA	2.4	–	V
Output "Low" Voltage (TTL)	V_{OL1}	I_{OL} = 1.200 mA	–	0.4	V
Output "High" Voltage (CMOS)	V_{OH2}	I_{OH} = 0.040 mA	0.9 V_{CC}	–	V
Output "Low" Voltage (CMOS)	V_{OL2}	I_{OL} = 0.040 mA	–	0.1 V_{CC}	V
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{CC}	–	0.001	mA
Supply Current (logic)	I_{CC}		6	12	mA

4.4 Timing Characteristics

Write Operation (Refer to Figure 11)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	t_{CYC}	1000	–	ns
Enable Pulse Width "High Level"	PW_{EH}	450	–	ns
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	25	ns
Address Set–up Time RS,R/W	t_{AS}	140	–	ns
Address Hold Time	t_{AH}	10	–	ns
Data Set–up Time	t_{DSW}	195	–	ns
Data Hold Time	t_{H}	10	–	ns

Read Operation (Refer to Figure 12)

Item	Symbol	Min	Max	Unit
Enable Cycle Time	t_{CYC}	1000	–	ns
Enable Pulse Width "High Level"	PW_{EH}	450	–	ns
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	25	ns
Address Set–up Time RS,R/W	t_{AS}	140	–	ns
Address Hold Time	t_{AH}	10	–	ns
Data Delay Time	t_{DDR}	–	320	ns
Data Hold Time	t_{DHR}	20	–	ns

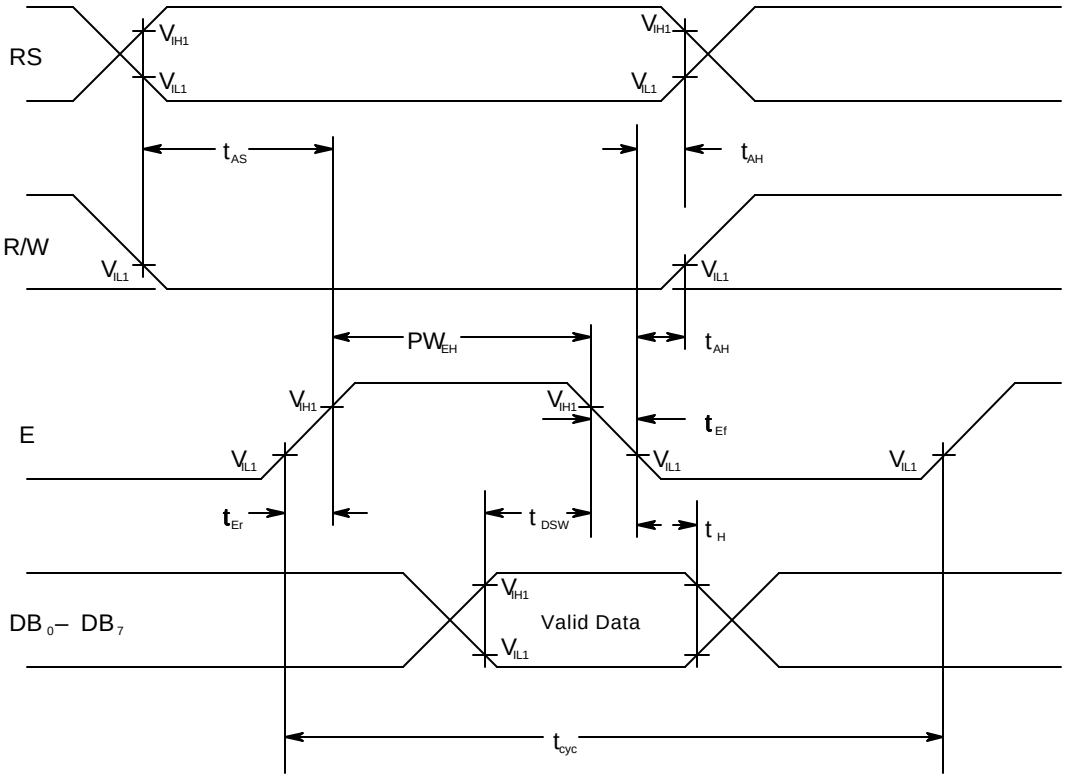

Figure 11 Interface Timing (Write)

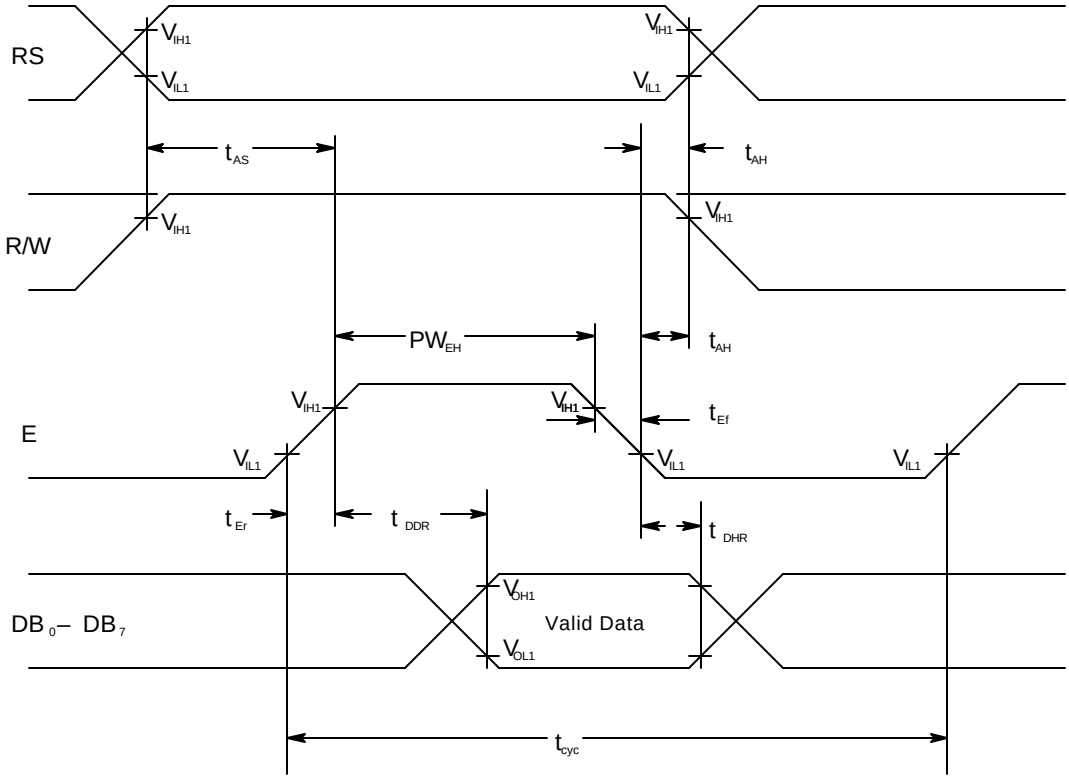

Figure 12 Interface Timing (Read)

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4.5 Timing Sequence for 8 Bit Parallel Interface

Figure 13 illustrates the typical Busy Flag check sequence for an 8 bit data interface.

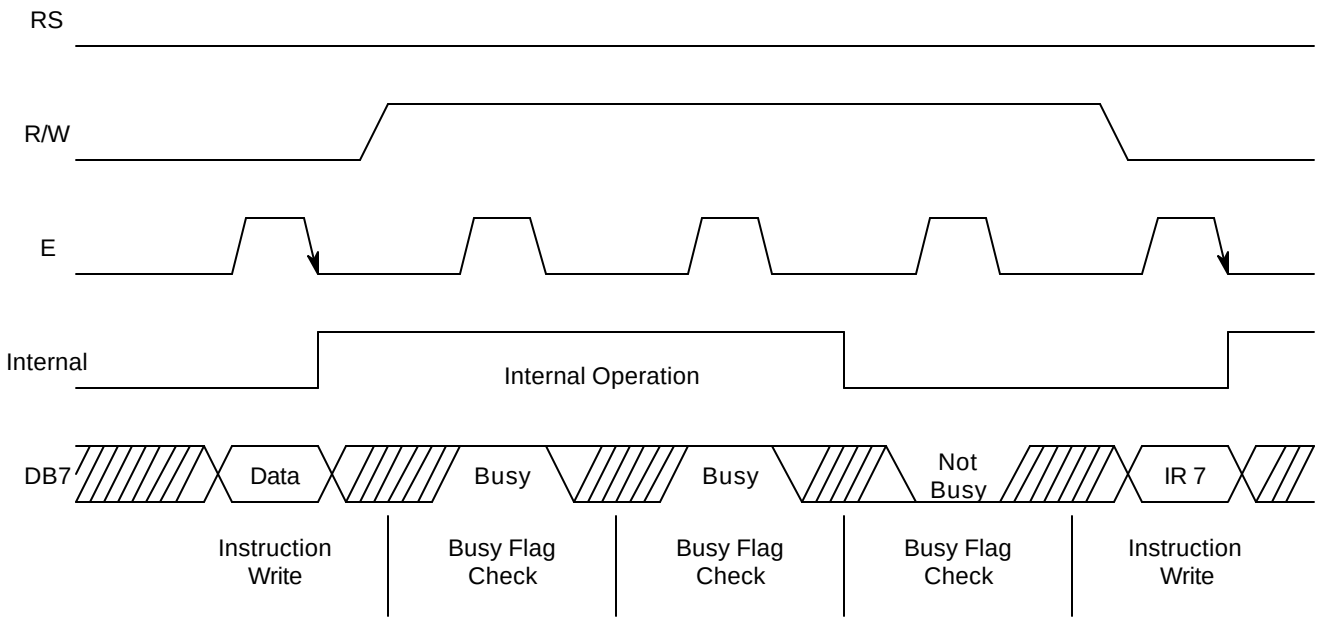


Figure 13 Busy Flag Check Sequence for 8–bit Parallel Interface

4.6 Timing Sequence for 4 Bit Parallel Interface

Figure 14 illustrates the typical Busy Flag check sequence for a 4 bit data bus interface.

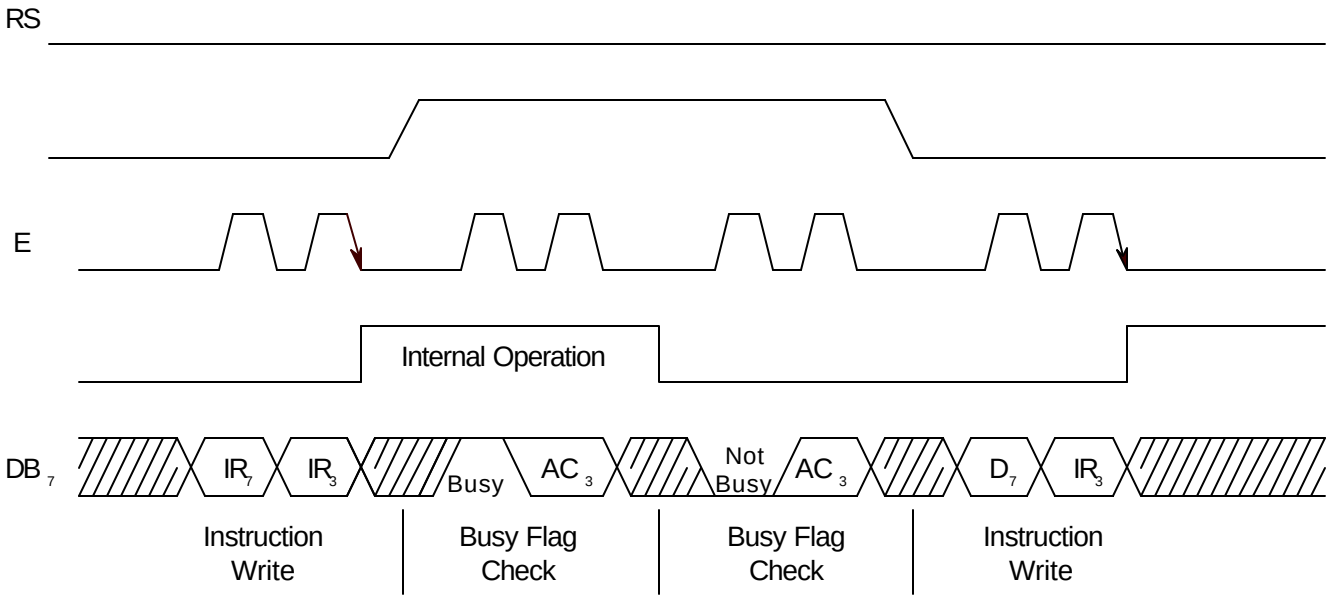


Figure 14 Busy Flag Check Sequence for 4–bit Parallel Interface

Note: IR_7, IR_3: Instruction, 7th bit & 3rd bit
AC_3: Address Counter, 3rd bit

4.7 Connector Pin Assignments (P1)

Pin No.	Function
1	N/C
2	V_{BIAS} (Factory Set–up Test Point)
3	N/C *
4	ADJ (Viewing Angle Adjustment)
5	R/W (Read = Logic 1)
6	Key (Pin Removed)
7	RS
8	Ground
9	Enable (E1)
10	Ground
11	DB_0
12	Ground
13	DB_1
14	Ground
15	DB_2
16	Ground
17	DB_3
18	Ground
19	DB_4
20	Ground
21	DB_5
22	V_{CC} ($+5V_{DC}$ – Parallel with Pin 24)
23	DB_6
24	V_{CC} ($+5V_{DC}$ – Parallel with Pin 22)
25	DB_7
26	N/C

* When the display module includes the serial data input option, Pin 3 is internally connected to provide signal E2 as an output to a second display module.

CMOS Note: Care must be taken to insure that input signals do not exceed the supply voltage or ground levels. Data cables must be as short as possible to reduce signal overshoots.

5.0 ENVIRONMENTAL CHARACTERISTICS

5.1 Operating

Temperature: –30 to +80°C

Humidity: (@ 40ºC) 95% RH (non–condensing)

Humidity (< 40°C): Absolute humidity must be lower the humidity of 95% RH at 40°C

Vibration: 10g at 10 to 400Hz (3 axes)

Shock: 10g (all axes)

5.2 Non–Operating

Temperature: –40°C to +85°C

6.0 OPTICAL SPECIFICATIONS

6.1 Optical Characteristics

Format:	Four lines of 20 characters
Character Font:	5x7 dot matrix with cursor
Character Height w/ cursor:	0.48" (12.1mm)
Character Height w/o cursor:	0.39" (9.9mm)
Character Width:	0.24" (6.1mm)
Overall Active Area:	5.70" x 2.34" (144.9mm x 59.5mm)
Peak Vertical Viewing Angle:	20° below normal plane
Viewing Mode:	Reflective, light field

Item	Symbol	Condition	Min	Typ	Max	Unit
Viewing Angle–Vertical	$\phi 1–\phi 2$	CR = 2.0, θ = 0°	100	120	–	deg.
Viewing Angle–Horizontal*	T	CR = 2.0	±45	±55	–	deg.
Contrast ratio (Peak)**	CR	25°C	10	18	–	–
Response time (ON)**	t_r	25°C	–	100	150	mS
		–30°C	–	2000	–	mS
Response time (OFF)**	t_f	25°C	–	150	200	mS
		–30°C	–	4000	–	mS

* Measured at peak vertical angle, ϕ = –20°

** Measured at peak viewing angles:

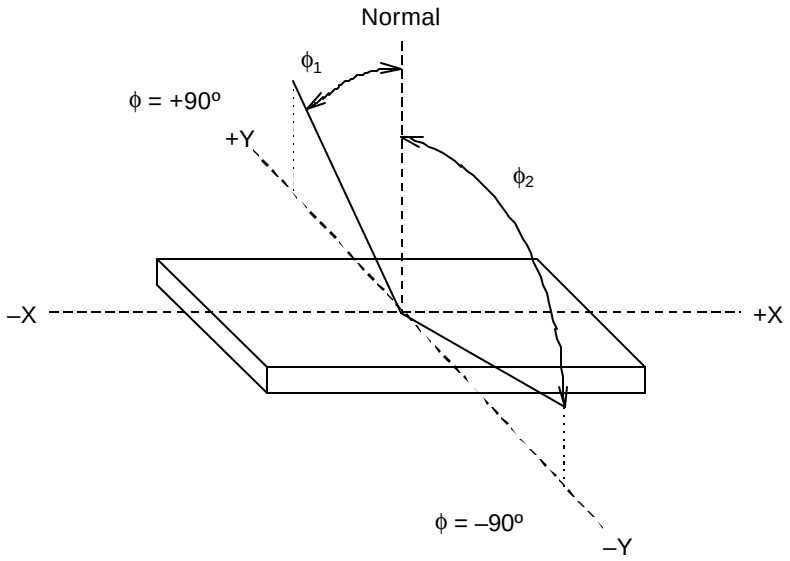


Figure 15 Definition of Vertical Viewing Angle

Definition of Horizontal Viewing Angle–top Viewing Display (for Bottom Viewing Displays ϕ = –20° Typically)

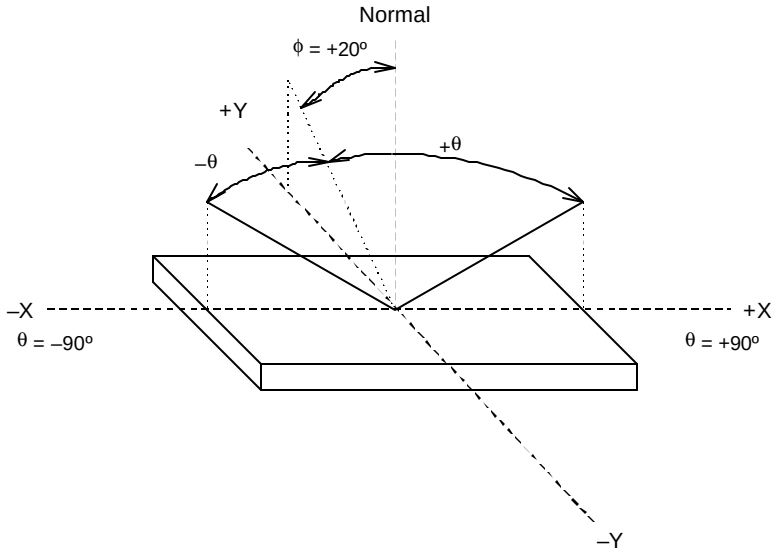


Figure 16 Definition of Horizontal Viewing Angle

Display contrast ratio is given by:

$$CR = \frac{B_2}{B_1}$$

Where: B_1 = Brightness of selected segment

B_2 = Brightness of non–selected segment

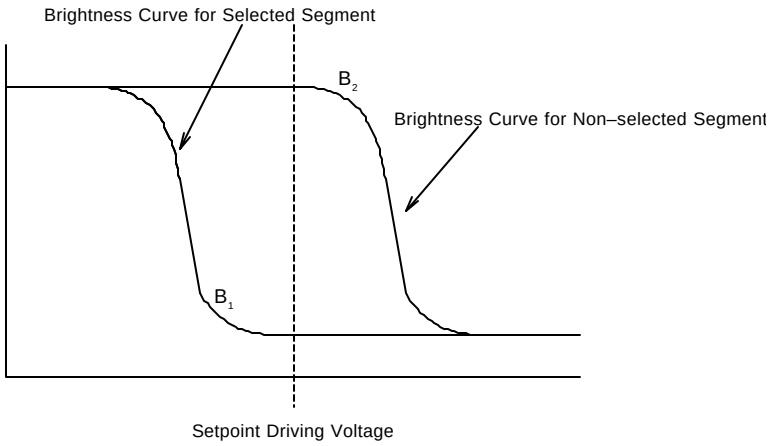


Figure 17 Definition of Contrast Ratio (CR)

Definition of optical response.

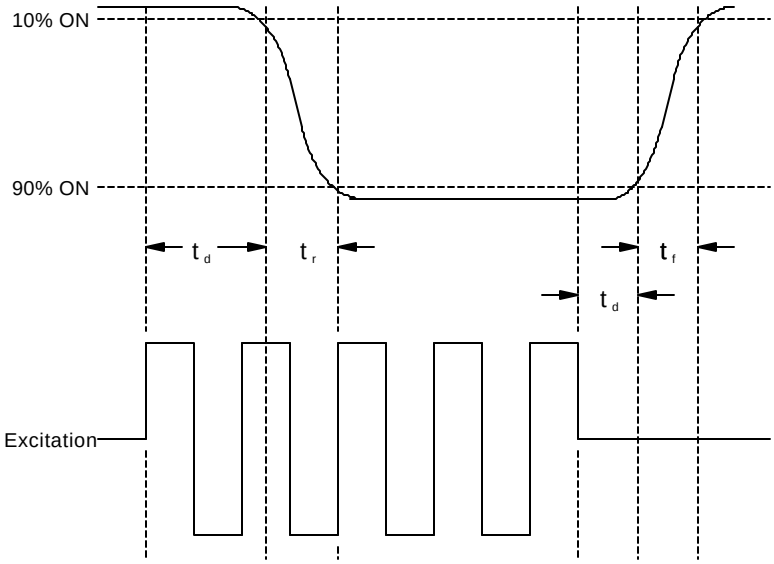


Figure 18 Definition of Optical Response

6.2 Viewing Angle Adjustment

The factory preadjusts the viewing angle of the display by setting the LCD bias voltage to 10.2 Volts using the on–board potentiometer. This is considered to be a nominal adjustment, but the user may prefer to vary this to optimize the viewing for a particular application. The bias voltage is measured between V_{CC} (pin #22) and V_{BIAS} (pin #2).

The viewing angle and contrast ratio may be externally controlled using an additional 10K ohm potentiometer. The potentiometer on the rear of the module must first be set to the maximum resistance by turning the adjustment fully counterclockwise. A 10K ohm potentiometer can then be connected between pin numbers 4 and 22 on the connector. Since the module has wide viewing angle characteristics and built–in temperature compensation of the viewing angle, the user may find that this external viewing control is unnecessary.

7.0 INSTALLATION NOTE

To protect the front polarizer from accidental damage it is highly recommended that the LCD be mounted behind a clear glass or polycarbonate window material. It is also recommended that an air gap of at least .030" to .050" minimum be provided between the window material and the surface of the LCD to prevent the transfer of static charges to the front surface of the LCD. Supertwist LCD's may activate un–driven elements in response to a surface static charge on the front polarizer. It may take several minutes for such a surface static charge to dissipate.

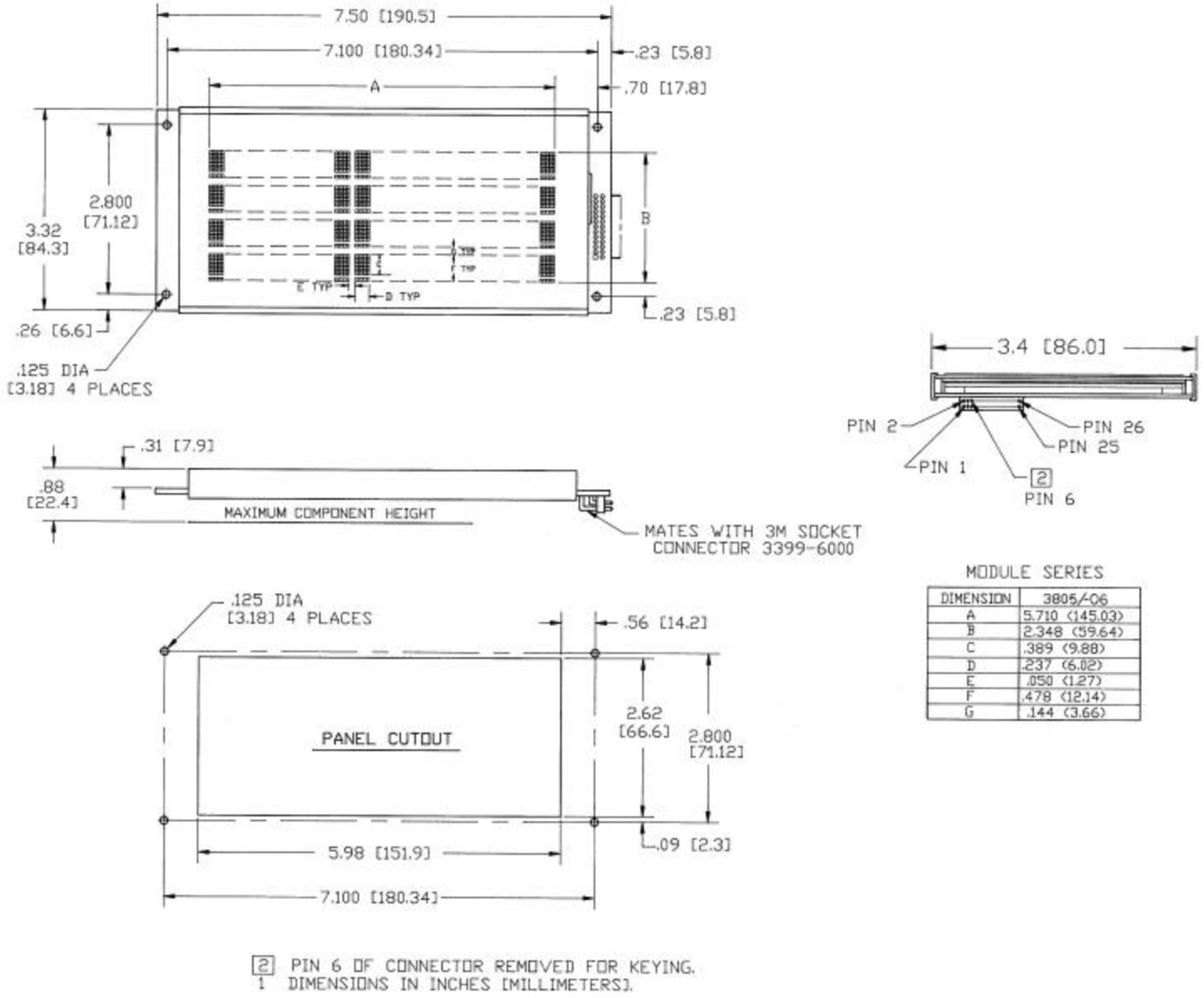
8.0 ACCESSORIES

Power/Data Connector Only (26 pin)	30554–99
Keyed Power/Data Connector with cable	30554–XX
Double ended keyed Power/Data cable(26 pin)	30553–XX

(XX = length in inches of cable)

(Standard cables are 18 and 36 inches)

9.0 OUTLINE AND INSTALLATION CHARACTERISTICS



MODULE SERIES

DIMENSION	3805/-06
A	5.710 (145.03)
B	2.348 (59.64)
C	.389 (9.88)
D	.237 (6.02)
E	.050 (1.27)
F	.478 (12.14)
G	.144 (3.66)

Figure 19 03805–06–0100 Outline Drawing